AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (previously presented) A semiconductor device comprising:

a circuit region on a semiconductor substrate;

a first guard ring extending into the substrate and surrounding said circuit region;

a second guard ring extending into the substrate between said circuit region and said first guard ring surrounding said circuit region; and

first connections extending into the substrate and connecting said first guard ring and said second guard ring to each other and dividing an area sandwiched between said first guard ring and said second guard ring into a plurality of subareas.

2. (original) A semiconductor device according to claim 1, wherein said circuit region has a corner, and said first connections connect a corner of said second guard ring which corresponds to the corner of said circuit region to said first guard ring.

3. (currently amended) A semiconductor device ~~according to claim 1~~ comprising:

a circuit region on a semiconductor substrate;

a first guard ring extending into the substrate and surrounding said circuit region;

a second guard ring extending into the substrate between said circuit region and said first guard ring surrounding said circuit region; and

first connections extending into the substrate and connecting said first guard ring and said second guard ring to each other and dividing an area sandwiched between said first guard ring and said second guard ring into a plurality of subareas,

wherein said circuit region has a corner, and said first connections are spaced at a density which is progressively greater toward the corner of said circuit region.

4. (currently amended) A semiconductor device ~~according to claim 1, further~~ comprising:

a circuit region on a semiconductor substrate;

a first guard ring extending into the substrate and surrounding said circuit region;

a second guard ring extending into the substrate between said circuit region and said first guard ring surrounding said circuit region;

first connections extending into the substrate and connecting said first guard ring and said second guard ring to each other and dividing an area sandwiched between said first

guard ring and said second guard ring into a plurality of subareas;

a third guard ring disposed between said second guard ring and said circuit region in surrounding relation to said circuit region; and

second connections connecting said second guard ring and said third guard ring to each other and dividing an area sandwiched between said second guard ring and said third guard ring into a plurality of subareas.

5. (original) A semiconductor device according to claim 4, wherein junctions where said first connections are connected to said second guard ring and junctions where said second connections are connected to said second guard ring are positioned out of alignment with each other.

6. (currently amended) A semiconductor device according to claim [[1]] 4, wherein ~~further comprising:~~

~~a third guard ring disposed between said second guard ring and said circuit region in surrounding relation to said circuit region; and~~

~~second connections connecting said second guard ring and said third guard ring to each other and dividing an area sandwiched between said second guard ring and said third guard ring into a plurality of subareas;~~

said second guard ring, said first connections, and said second connections are connected to each other at junctions

where the number of connected linear patterns extending in different directions therefrom is 3.

7. (currently amended) A semiconductor device ~~according to claim 1~~ comprising:

a circuit region on a semiconductor substrate;

a first guard ring extending into the substrate and surrounding said circuit region;

a second guard ring extending into the substrate between said circuit region and said first guard ring surrounding said circuit region; and

first connections extending into the substrate and connecting said first guard ring and said second guard ring to each other and dividing an area sandwiched between said first guard ring and said second guard ring into a plurality of subareas,

wherein said circuit region comprises a first insulating film having a dielectric constant lower than an oxide film and a second insulating film stacked on said first insulating film and different in film quality from said first insulating film, and said second guard ring covers sides of said first insulating film and a slit between said first insulating film and said second insulating film.

8. (original) A semiconductor device according to claim 7, wherein said first insulating film comprises at least one of a ladder-type hydrogenated siloxane film, a hydrogen-containing

polysiloxane film, an SiOC film, an SiOF film, an SiC film, and an organic film.

9. (original) A semiconductor device according to claim 4, wherein said circuit region has a corner, and said second connections connect a corner of said third guard ring which corresponds to the corner of said circuit region to said second guard ring.

10. (original) A semiconductor device according to claim 4, wherein said circuit region has a corner, and said second connections are spaced at a density which is progressively greater toward the corner of said circuit region.

11. (original) A semiconductor device according to claim 4, wherein said circuit region comprises a first insulating film having a dielectric constant lower than an oxide film and a second insulating film stacked on said first insulating film and different in film quality from said first insulating film, and said third guard ring covers sides of said first insulating film and a slit between said first insulating film and said second insulating film.

12. (original) A semiconductor device according to claim 11, wherein said first insulating film comprises at least one of a ladder-type hydrogenated siloxane film, a hydrogen-containing polysiloxane film, an SiOC film, an SiOF film, an SiC film, and an organic film.

13. (previously presented) A semiconductor device comprising:

a semiconductor substrate having a circuit region therein;

an insulating layer on said semiconductor substrate;

a first guard ring in said insulating layer and surrounding said circuit region;

a second guard ring in said insulating layer between said circuit region and said first guard ring and surrounding said circuit region; and

first connections that are in said insulating layer and connecting said first guard ring and said second guard ring to each other to divide an area sandwiched between said first guard ring and said second guard ring into a plurality of subareas.

14. (previously presented) The semiconductor device of claim 13, further comprising a third guard ring between said second guard ring and said circuit region and surrounding said circuit region, and second connections connecting said second guard ring and said third guard ring to each other and dividing an area sandwiched between said second guard ring and said third guard ring into a plurality of subareas.

15. (previously presented) The semiconductor device of claim 14, wherein junctions where said first connections are connected to said second guard ring and junctions where said

second connections are connected to said second guard ring are out of alignment with each other.

16. (previously presented) The semiconductor device of claim 14, wherein said second guard ring, said first connections, and said second connections are connected to each other at junctions where the number of connected linear patterns is different directions therefrom is three.

17. (previously presented) A semiconductor device comprising:

a semiconductor substrate having a circuit region therein;

a first guard ring surrounding said circuit region;

a second guard ring between said circuit region and said first guard ring and surrounding said circuit region, said second guard ring being spaced from said first guard ring and not overlapping said first guard ring when viewed from a direction perpendicular to a surface of said substrate; and

first connections connecting said first guard ring and said second guard ring to each other.

18. (previously presented) The semiconductor device of claim 17, further comprising a third guard ring between said second guard ring and said circuit region and surrounding said circuit region, and second connections connecting said second guard ring and said third guard ring to each other and dividing

an area sandwiched between said second guard ring and said third guard ring into a plurality of subareas.

19. (previously presented) The semiconductor device of claim 18, wherein junctions where said first connections are connected to said second guard ring and junctions where said second connections are connected to said second guard ring are out of alignment with each other.

20. (previously presented) The semiconductor device of claim 18, wherein said second guard ring, said first connections, and said second connections are connected to each other at junctions where the number of connected linear patterns is different directions therefrom is three.